Section II. (Amendments to Claims)

Please amend claims 1,

1. (Currently amended) A microelectronic structure comprising:

at least one layer of high dielectric constant material comprising amorphous dielectric metal oxide having: (i) a voltage independent capacitance, (ii) a capacitance density of from about 1000 to about 10,000 nF/cm^2, and (iii) a current leakage of $<10^{-7}$ A/cm^2;

at least one conductive barrier layer in contact with the layer of high dielectric constant material, wherein such conductive barrier layer comprises at least one material selected from the group consisting of Pt, Ir, IrO_2, Ir_2O_3, Ru, RuO_2, TaN, NbN, HfN, ZrN, WN, W_2N, TiN, TiSiN, TiAlN, TaSiN, NbAlN, and compatible combinations, mixtures and alloys thereof;

at least one metal layer in contact with the conductive barrier layer, wherein said metal layer comprises metal or metal alloy including a material selected from the group consisting of Cu and Al;

wherein said at least one conductive barrier layer is between said at least one layer of high dielectric constant material and said at least one metal layer;

~~wherein when said material of said at least one metal layer is Al, said at least one material of said conductive barrier layer is not Ir or IrO_2.~~

2. (Currently amended) A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises at least one material selected from the group consisting of TaN, NbN, HfN, ZrN, WN, W_2N, TiN, TiSiN, TiAlN, TaSiN, and NbAlN.

3. (Original) A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises TiAlN.

4. (Original) A microelectronic structure according to claim 1, wherein said metal layer comprises Cu or Cu alloy.

5. (Original) A microelectronic structure according to claim 1, wherein said metal layer comprises Al or Al alloy.

6. (Currently amended) A microelectronic structure according to claim 1, wherein said ~~layer of high dielectric constant material comprises a complex~~ amorphous dielectric metal oxide is selected from the group consisting of $SrBi_2Ta_2O_9$ (SBT), $(Ba,Sr)TiO_3$ (BST), $BiTaO_4$ (BT), $Bi_4Ti_3O_{12}$, barium titanate, strontium titanate, barium strontium titanate, strontium bismuth tantalate, bismuth titanate, and lead zirconium titanate ~~and Pb(Zr,Ti)O$_3$ (PZT)~~.

7. (Currently amended) A microelectronic structure according to claim 1, wherein said layer of high dielectric constant material comprises amorphous SBT ~~perovskite BST~~ material.

8. (Original) A microelectronic structure according to claim 1, wherein said layer of high dielectric constant material comprises amorphous BST material.

9. (Original) A microelectronic structure according to claim 1, wherein said conductive barrier layer has a thickness in a range of from about 1nm to about 100nm.

10. (Original) A microelectronic structure according to claim 1, wherein said conductive barrier layer has a thickness in a range of from about 5nm to about 20nm.

11. (Original) A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises Pt.

12. (Original) A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises Ir.

13. (Original) A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises IrO_2.

14. (Original) A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises Ru.

15. (Original) A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises RuO_2.

16. (Original) A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises TiAlN.

17. (Original) A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises TaN.

18. (Original) A microelectronic structure according to claim 1, comprising a first conductive barrier layer and a second conductive barrier layer, wherein the first conductive barrier layer is in contact with the layer of high dielectric constant material, and the second conductive barrier layer overlies said first conductive barrier layer and is in contact with the metal layer.

19. (Original) A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Pt, and said second conductive barrier layer comprises IrO_2.

20. (Original) A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Pt, and said second conductive barrier layer comprises TiAlN.

21. (Original) A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Pt, and said second conductive barrier layer comprises Ir.

22. (Original) A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Ir, and said second conductive barrier layer comprises IrO_2.

23. (Original) A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Ir, and said second conductive barrier layer comprises TiAlN.

24. (Original) A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises IrO_2, and said second conductive barrier layer comprises Ir.

25. (Original) A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises IrO_2, and said second conductive barrier layer comprises TiAlN.

26. (Original) A microelectronic structure according to claim 1, comprising a first conductive barrier layer, a second conductive barrier layer, and a third conductive barrier layer, wherein said first conductive barrier layer is in contact with the layer of high dielectric constant material, said second conductive barrier layer overlies said first conductive barrier layer, and said third conductive barrier layer overlies said second conductive barrier layer and is in contact with the metal layer.

27. (Currently amended) A microelectronic structure comprising:

at least one layer of high dielectric constant material;

~~at least one conductive barrier layer in contact with the layer of high dielectric constant material, wherein such conductive barrier layer comprises at least one material selected from the group consisting of Pt, Ir, IrO_2, Ir_2O_3, Ru, RuO_2, TaN, NbN, HfN, ZrN, WN, W_2N, TiN, TiSiN, TiAlN, TaSiN, NbAlN, and compatible combinations, mixtures and alloys thereof~~ a first conductive barrier layer comprising IrO_2, a second conductive barrier layer comprising Ir_2O_3, and a third conductive barrier layer comprising Ir, wherein said first conductive barrier layer is in contact with the layer of high dielectric constant material, said second conductive barrier

layer overlies said first conductive barrier layer, and said third conductive barrier layer overlies said second conductive barrier layer;

at least one metal layer in contact with the third conductive barrier layer, wherein said metal layer comprises metal or metal alloy including a material selected from the group consisting of Cu or and Al;

wherein said ~~at least one~~ first, second and third conductive barrier layers are ~~layer is~~ between said at least one layer of high dielectric constant material and said at least one metal layer~~;~~

~~wherein said at least one conductive barrier layer is between said at least one layer of high dielectric constant material and said at least one metal layer;~~

~~wherein when said material of said at least one metal layer is Al, said at least one material of said conductive barrier layer is not Ir or IrO_2;~~

~~comprising a first conductive barrier layer, a second conductive barrier layer, and a third conductive barrier layer, wherein said first conductive barrier layer is in contact with the layer of high dielectric constant material, said second conductive barrier layer overlies said first conductive barrier layer, and said third conductive barrier layer overlies said second conductive barrier layer and is in contact with the metal layer,~~

~~wherein said first conductive barrier layer comprises IrO_2, said second conductive barrier layer comprises Ir_2O_3, and said third conductive barrier layer comprises Ir~~.

28. (Currently amended) A microelectronic structure according to claim 1, comprising:

~~at least one layer of perovskite BST material;~~

a first conductive barrier layer in contact with the ~~layer of perovskite BST material,~~ layer of high dielectric constant material and comprising Pt;

a second conductive barrier layer overlaying said first conductive barrier layer, and comprising Ir~~; and~~

~~at least one metal layer in contact with said second conductive barrier layer, comprising Cu or Cu alloy~~.

29. (Original) A microelectronic structure according to claim 1, comprising:

at least one layer of amorphous BST material;

a conductive barrier layer in contact with the layer of amorphous BST material, comprising at least one material selected from the group consisting of Ir, Ru, RuO_2, and IrO_2;

at least one metal layer in contact with the conductive barrier layer, comprising Cu or Cu alloy.

30. (Original) A microelectronic structure according to claim 1, comprising:

at least one layer of amorphous SBT material;

a conductive barrier layer in contact with the layer of amorphous SBT material, comprising at least one material selected from the group consisting of Ir, Ru, TaN and TiAlN;

at least one metal layer in contact with the conductive barrier layer, comprising Cu or Cu alloy.

31. (Currently amended) A microelectronic structure according to claim 1, comprising:

at least one layer of amorphous lead zirconium titanate ~~PZT~~ material;

a conductive barrier layer in contact with the layer of amorphous lead zirconium titanate ~~PZT~~ material, comprising at least one material selected from the group consisting of Ir, Ru, RuO_2, and IrO_2;

at least one metal layer in contact with the conductive barrier layer, comprising Cu or Cu alloy.

32. (Original) A microelectronic structure according to claim 1, comprising a capacitor structure selected from the group consisting of stack capacitors and trench capacitors.

33. (Original) A microelectronic structure according to claim 1, comprising a memory cell integrated circuit structure.

34. (Original) A microelectronic structure according to claim 33, wherein the memory cell integrated circuit structure comprises a non-volatile memory cell integrated circuit structure.

35. (Original) A microelectronic structure according to claim 33, wherein the memory cell integrated circuit structure comprises a dynamic random access memory cell integrated circuit structure.

36. (Original) A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises a decoupling circuit.

37. (Original) A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises an impedance matching circuit.

38. (Original) A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises an analog circuit component.

39. (Original) A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises an active circuit element selected from the group consisting of electrically tunable capacitor, sensor, and microelectromechanical machine (MEMS).